What is Claimed is:

[c1] A memory cell formed on a substrate, comprising:

first and second fully depleted transfer devices each having a body region and first and second diffused electrodes, and

a differential storage capacitor having at least one node abutting and in electrical contact with one of said first and second diffused electrodes of each of said transfer devices, said storage capacitor having a primary capacitance and a plurality of inherent capacitances, wherein said primary capacitance has a capacitive value that is at least approximately five times greater than that of said plurality of inherent capacitances.

[c2] The memory cell in claim 1, wherein said transfer devices have channel regions that extend substantially through said body regions.

[c3] The memory cell of claim 1, wherein the substrate comprises a SOI substrate having a buried insulator layer.

[c4] The memory cell of claim 3, wherein said body regions are disposed on and contact said buried insulator layer.

[c5] The memory cell of claim 2, wherein said transfer devices each have gate electrodes that substantially surround respective channel regions.

[c6] The memory cell of claim 1, wherein said first diffused electrode of said first transfer device, said body region of said first transfer device, said second diffused electrode of said first transfer device, and a portion of said first node of said differential storage capacitor are all disposed in sequence on a first rail of semiconductor material.

[c7] The memory cell of claim 6, wherein said first rail of semiconductor material is selected from the group consisting of Group III-V semiconductor materials and alloys thereof, silicon, germanium, and Si-Ge alloys.

[c8] The memory cell of claim 1, wherein said transfer device has a gate electrode and a first dielectric disposed on said body region, and said differential storage capacitor has a plate electrode and a second dielectric disposed on said first

node.

[c9] The memory cell of claim 8, wherein said first dielectric has a dielectric constant that is different from that of said second dielectric.

[c10] The memory cell of claim 6, wherein said first diffused electrode of said second transfer device, said body region of said second transfer device, said second diffused electrode of said second transfer device, and a remaining portion of said first node of said differential storage capacitor are all disposed in sequence on a second rail of semiconductor material disposed adjacent said first rail of semiconductor material.

[c11] The memory cell of claim 10, wherein said differential storage capacitor has a dielectric that covers a portion of said first rail of semiconductor material in which said first node is disposed.

[c12] The memory cell of claim 11, wherein said differential storage capacitor further comprises a plate electrode disposed over and bridging between both of said dielectric and an adjacent portion of said second rail of semiconductor material in which said remaining portion of said first node of said differential storage capacitor is disposed.

[c13] The memory cell of claim 12, wherein said dielectric is disposed between said plate electrode and said portion of said second rail of semiconductor material in which said remaining portion of said first node of said differential storage capacitor is disposed.

[c14] The memory cell of claim 13, further comprising a second capacitor dielectric disposed over said plate electrode, and a third capacitor electrode disposed on said second capacitor dielectric.

[c15] The memory cell of claim 14, wherein a portion of said third capacitor electrode contacts a portion of said first and second rails of semiconductor material.

[c16] A differential DRAM cell, comprising a plurality of rails of semiconductor material formed on a semiconductor substrate, each rail having source and drain diffusions therein separated by respective fully depleted channel regions

that are controlled by a gate electrode to form a transistor, each of said drain diffusions being coupled to a first node of a differential capacitor disposed on adjacent ones of said plurality of rails, at least one of said adjacent ones of said plurality of rails having a storage dielectric disposed on said first node, and a plate electrode of said differential capacitor being disposed on said storage dielectric.

[c17] A method of forming a memory cell, comprising:

forming rails of semiconductor material on a substrate;

doping a first portion of said rails;

forming a dielectric on said first portion of at least every other one of said rails;

forming a plate electrode on said first portion of adjacent pairs of said rails;

forming an FET in a second portion of said rails adjacent said first portion, said FET having a gate electrode disposed on all exposed sides of a part of said second portion of said rails.

[c18] The method of claim 17, wherein said comprises a SOI substrate having a buried insulator layer, and wherein said plurality of rails are disposed on and contact said buried insulator layer.

[c19] The method of claim 17, wherein dielectric is formed on said first portions of all of said rails on which a memory cell is to be formed.

[c20] The method of claim 19, wherein said rails have a height of at least approximately 0.15 microns.